L Number	Hits	Search Text	DB	Time stamp
1	8396	"etch stop" or "etch-stop"	USPAT; US-PGPUB	2003/05/15 13:44
2	722	"timed etch" or "time-etch"	USPAT; US-PGPUB	2003/05/15 13:44
3	65	("etch stop" or "etch-stop") with ("timed etch" or "time-etch")	USPAT; US-PGPUB	2003/05/15 13:44
4	411111	semiconductor or "integrated circuit"	USPAT; US-PGPUB	2003/05/15 13:45
5	63	(("etch stop" or "etch-stop") with ("timed etch" or "time-etch")) and (semiconductor or "integrated circuit")	USPAT; US-PGPUB	2003/05/15 13:45
6	1296227	metal or conductor	USPAT; US-PGPUB	2003/05/15 13:46
7	21	("timed etch" or "time-etch") with (metal or conductor)	USPAT; US-PGPUB	2003/05/15 13:46

EAST Browser - L7: (21) 2 with 6 | US 20020155693 A1 | Tag: 5 | Doc: 3/21 (ISOLATED) | Format : KWIC

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DOCUMENT-IDENTIFIER: US 20020155693 A1

TITLE: Method to form self-aligned anti-via interconnects

--------- KWIC --------

Detail Description Paragraph - DETX (5):

[0019] An etch stop layer 62 is deposited overlying the first metal layer 58. The purpose of the etch stop layer 62 is to allow complete etching through of the second metal layer 66 without damaging the underlying first metal layer 58. The etch stop layer 62 preferably comprises one of the group of: titanium nitride (TiN), titanium (T), tungsten (W), tungsten nitride (WN), tantalum (Ta), and tantalum nitride (TaN). The etch stop layer 62 is optional to the present invention. In the case where the etch stop layer 62 is not used, a timed etch must be used to allow independent etching of the first and second metal layers.

Claims Text - CLTX (5):

4. The method according to claim 1 wherein said step of etching partially through said metal layer to form vias comprises a timed etch.

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re it would have been obvious do eliminate it as long as you eliminate the function.

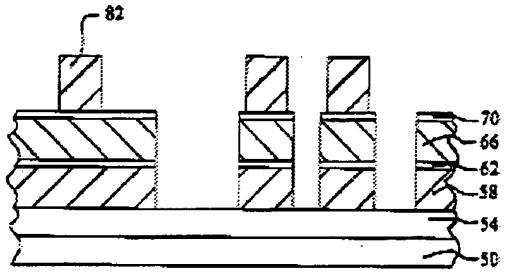

FIG. 5

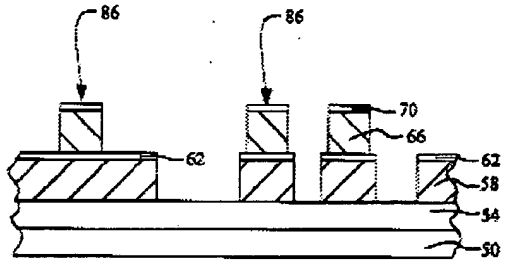

FIG. 6